JITTER REDUCTION IN ATM NETWORKS

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Abstract

Waiting time jitter is one of the main problems encountered in ATM networks as its amplitude (after filtering) can exceed those permitted by current standards.

This document puts forward a method for reducing jitter which consists in transmitting the phase information from the plesiochronous source measured by a reference clock. This information is protected against transmission errors and cell loss.

The results of the study show that it is possible to conform to CCITT recommendation G.823 for all plesiochronous rates of the 2 Mbit/s hierarchy defined in recommendation G.702 by using as the reference clock either the 2 MHz synchronisation network or the future 155 MHz network provided by the synchronous systems (SDH).

1. INTRODUCTION

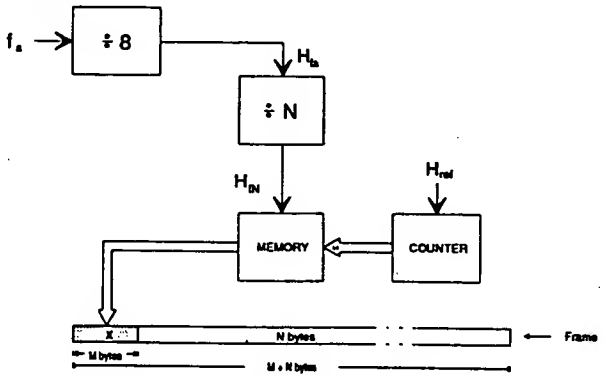
The method for reducing jitter proposed in the present document uses a reference clock common to both ends. The plesiochronous source phase is measured by the reference clock and the phase information is transmitted within one or more cells in the SAR-SDU field of the AAL - type 1 layer.

The plesiochronous rates used to calculate jitter were those defined in CCITT recommendation G.702 [1]. Several different frequencies, 2, 8, 34, 140 and 155 MHz, were used as the reference clock. In all cases studied, jitter amplitudes were lower than those considered in recommendation G.823 [2].

This document is divided into 5 chapters. Chapter 2 summarises the method proposed. Chapter 3 gives the expressions obtained to represent jitter and jitter shape before and after filtering through a low-pass filter. The method for protecting phase information against transmission errors and cell loss is presented in chapter 4.

2. METHOD

Figure 1 is a schematic diagram illustrating the method at the transmitting end. The phase information of the plesiochronous source (X) measured by the reference clock (H_{Tef}) and the associated data are transmitted within one or more cells in the SAR-SDU field of the AAL - type 1 layer (cf CCITT recommendation I.363, under approval).



f_a : plesiochronous source rate

H_{ref} : reference clock

X : number of times that $1/H_{ref}$ is contained in $1/H_{IN}$

Figure 1 : Schematic diagram of the method at the transmitting end.

The value of M is selected according to the value of X. The value of N is selected depending on how easily the frequency divider can be implemented and in such a way that M + N can be divided by 47.

In a CCITT meeting France proposed that a 2-bytes field should be reserved to send the value X every 16 cells, indicated by the cell number counter (SN) of the SAR layer returning to 0. Thus let's take M = 2 bytes and N = 750 bytes.

At the receiving end the information (X) is saved in a FIFO memory and compared with the output at a counter which is activated by the same reference clock as the one used at the transmitting end (H_{Tef}). Each time there is equality a pulse is generated. The mean pulse period is N bytes. Figure 2 shows the schematic diagram of the method at the receiving end.

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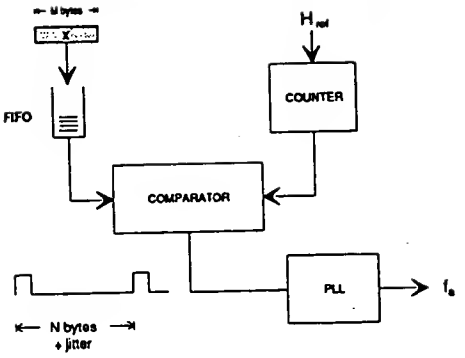


Figure 2 : Schematic diagram of the method at the receiving end.

3. JITTER REPRESENTATION

The jitter considered in this study is jitter resulting from phase differences between the plesiochronous signal (f_a) and the reference clock (H_{ref}), and without jitter at the input.

Signal H_{fN} is the frequency of N bytes. Referring to figure 1, it can be represented by :

$$H_{fN} = \frac{H_{fa}}{N} = \frac{f_a}{8N} \qquad (1)$$

The number of times that the reference clock is contained in the frame is :

$$X = \frac{H_{ref}}{H_{fN}} = 8N \frac{H_{ref}}{f_a} \qquad (2)$$

The value of the counter is represented by :

$$EX = \text{floor}(X) = \text{floor}\left(8N \frac{H_{ref}}{f_a} \right) \qquad (3)$$

floor (z) :the largest integer less than or equal to z

and the frame period (T_a) is :

$$T_m = 8N \frac{1}{f_a} \qquad (4)$$

If f_a and H_{ref} are stable, i.e. no jitter or variation, jitter results from the difference in phase between f_a and H_{ref} and its value peak-to-peak (p-p) in unit intervals (ui) is represented by :

of H_{ref}

$$g(p\text{-}p) = \frac{f_a}{H_{ref}} \qquad (5)$$

In this case, the periodic form of the jitter will depend on the phase difference between the two signals due to the asynchronism. The counter will take two values EX and EX + 1. The mean value will be X.

On the other hand, if the two signals vary according to their frequency tolerance, which is what happens in reality, jitter will result from the instantaneous phase difference between the two signals (as in the above case) and the variation in frequency of the two signals.

If "p" and "q" are the relative variations of f_a and H_{ref} respectively the values of X will vary within the limits represented by X_{max} and X_{min}

$$X_{max} = 8N \frac{H_{refo}}{f_{ao}} \frac{1 + q}{1 - p} \qquad (6)$$

$$X_{min} = 8N \frac{H_{refo}}{f_{ao}} \frac{1 - q}{1 + p} \qquad (7)$$

f_{ao} : mean rate of the plesiochronous source
H_{refo} : mean frequency of the reference clock

with a mean value $X_0 = 8N(H_{refo}/f_{ao})$.

The counter values will vary between $EX_{max} + 1$ and EX_{min}.

$$EX_{max} = \text{floor}(X_{max}) \qquad (8)$$

$$EX_{min} = \text{floor}(X_{min}) \qquad (9)$$

This variation may thus be represented by :

$$dEX = EX_{max} + 1 - EX_{min} \qquad (10)$$

Jitter in ui resulting from the frequency variations of the two signals is represented by :

$$g(p\text{-}p) = dEX \frac{f_{ao}}{H_{refo}} \qquad (11)$$

COMMENTS :

1 - With a 2.048 MHz ± 50 ppm reference clock :

* If the plesiochronous source is 2.048 MHz (± 50 ppm) the counter value will vary between $EX_0 - 1$ and $EX_0 + 1$ (2 ui) with $EX_0 = 6000$ (EX_0 : integer mean value of EX, see expression (15)).

* If other plesiochronous sources are used (8, 34 or 140 Mbit/s) the counter value will only vary between EX_0 and $EX_0 + 1$. However, peak-to-peak jitter will be about 4, 16 and 68 ui for the 8, 34 and 140 Mbit/s sources respectively.

2 - With a 155.52 MHz reference clock :

* EX will vary more, especially for 2 and 8 Mbit/s sources. However, peak-to-peak jitter in ui will be much smaller than in the above case.

3 - Since the counter takes a limited number of values around EX_0, only the difference with EX_0 can be transmitted instead of the value itself.

3.1 Jitter representation in the time domain

Signals f_a and H_{ref} vary within their tolerance limits (this variation is usually very slow). As a result, the values X, EX and T_a defined in expressions (2), (3) and (4) will also vary.

If the integer mean value of EX is defined as follows :

$$EX_o = \text{floor}\left(8N \frac{H_{refo}}{f_{ao}} \right) \qquad (12)$$

the variation of EX in relation to the mean value EX_0 will be :

$$dX = EX - EX_o \qquad (13)$$

Note that dX is different from dEX as defined in (10) as dX represents the variation of the counter each time N bytes is read (in relation to the mean value of EX), while dEX represents the maximum variation of EX. Thus, the maximum value of dX is dEX/2.

To represent jitter signal in the time domain, phase difference between the frame period (T_a) and the period represented by EX times the reference clock (EX/H_{ref}) must be determined.

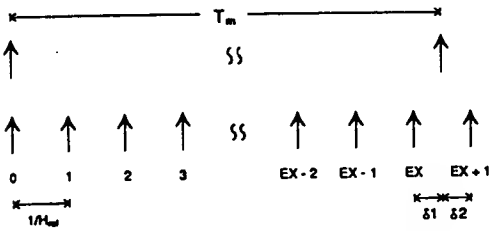


Figure 3 : Phase difference between EX/H_{ref} and T_m

The phase differences are represented by (see figure 3) :

$$\delta 1 = T_m - EX \frac{1}{H_{ref}} \qquad (14)$$

$$\delta 2 = \frac{1}{H_{ref}} - \delta 1 \qquad (15)$$

Let's calculate T_0, the mean time it takes the phase difference to come back to its initial value (it means the counter changes value, e.g. from EX_0 to $EX_0 + 1$). This is illustrated in figure 4.

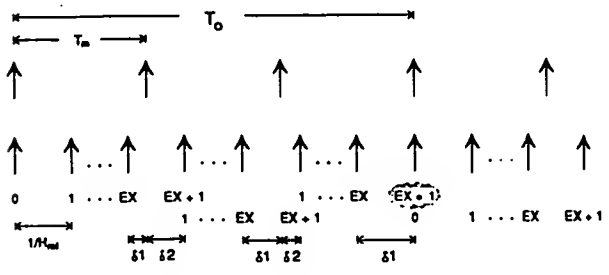


Figure 4 : Variation in phase difference between EX/H_{ref} and T_m

It can be seen from figure 4 that phase difference δ1 increases while δ2 decreases.

The same demonstration can be used when δ1 decreases and δ2 increases. In our example the initial value of δ1 is smaller than δ2 and its value is $1/3(1/H_{ref})$. It can be observed that $T_0 = 3T_a$. There is thus a relation between T_0 and the initial value of δ1.

$$T_o = \frac{\frac{1}{H_{ref}}}{\delta 1} T_m = \frac{\frac{1}{H_{ref}}}{\frac{1}{3}\frac{1}{H_{ref}}} T_m = 3\ T_m \qquad (18)$$

The relative value of phase difference can be represented by :

$$\rho = \frac{\delta 1}{\frac{1}{H_{ref}}} \qquad (17)$$

Thus, the value of T_0 represented in (18) is as follows :

$$T_o = \frac{1}{\rho}\ T_m \qquad (19)$$

The phenomenon is analogous to a justification process with "ρ" as the justification rate, i.e. if ρ = h/k (h and k being prime numbers) the counter value will change from EX_0 to $EX_0 + 1$ (if δ1 < δ2) "h" number of times during "k" T_a periods.

The values of T_0 and ρ represented by (16) and (17) can be also calculated with δ2 instead of δ1 if δ2 < δ1.

Waiting time jitter is represented by [4] :

$$\phi(t) = \rho t - \text{floor}[\rho\ \text{floor}(t)] \qquad (19)$$

The slope is represented by "ρ t" and the justification by floor[ρ floor(t)].

Expression (19) can be used to represent jitter resulting from phase differences between f_a and H_{ref}. The expressions which represent jitter in ui vary according to the values of δ1 and δ2 (δ1 < δ2 or δ1 > δ2).

Thus the following expressions are obtained :

a) δ1 < δ2

$$\phi(t) = \frac{f_a}{H_{ref}}\left(dX + \rho t - \text{floor}[\rho\ \text{floor}(t)]\right) \qquad (20)$$

b) δ2 < δ1

$$\phi(t) = \frac{f_a}{H_{ref}}\left(dX + 1 - \rho t + \text{floor}[\rho\ \text{floor}(t)]\right) \qquad (21)$$

A number of calculations were performed with the aid of expressions (20) and (21). Figure 5 shows jitter for three different signals. It shows jitter resulting from the phase difference of signals f_a and H_{ref} (see curves a, b and c) and jitter resulting from the frequency variation of the two signals (from a to b and b to c). Note that in reality jitter does not vary abruptly from one level to another since the frequency variation of the signals is not instantaneous as depicted in the simulation.

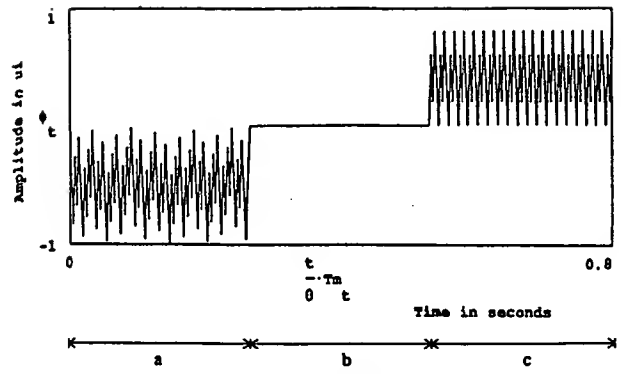


Figure 5 : Jitter in ui for :

a - H_{ref} = 2,048 (1 - 50 x 10^{-6}) MHz f_a = 2,048 (1 + 20 x 10^{-6}) Mbit/s
b - H_{ref} = f_a (jitter = 0)
c - H_{ref} = 2,048 (1 + 50 x 10^{-6}) MHz f_a = 2,048 (1 - 50 x 10^{-6}) Mbit/s

The value of θ is used to modify graphics resolution. Variable t must therefore be replaced by (t/θ) in expressions (20) and (21). On the other hand, note that time (t) in expressions (20) and (21) is normalised in comparison with T_a.

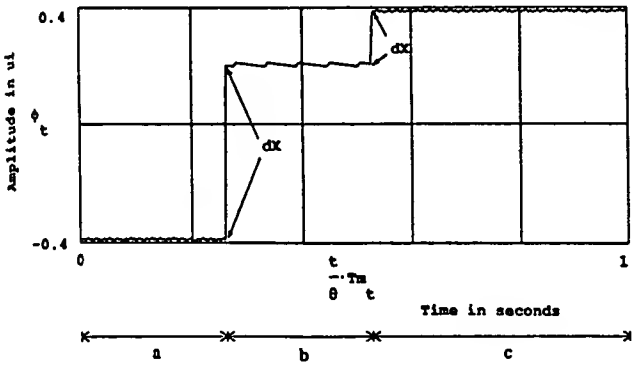


Figure 6 : Jitter in ui for :

a - H_{ref} = 155,52 (1 - 15 x 10^{-6}) MHz f_a = 2,048 (1 + 50 x 10^{-6}) Mbit/s
b - H_{ref} = 155,52 (1 - 15 x 10^{-6}) MHz f_a = 2,048 (1 - 50 x 10^{-6}) Mbit/s
c - H_{ref} = 155,52 (1 + 15 x 10^{-6}) MHz f_a = 2,048 (1 - 50 x 10^{-6}) Mbit/s

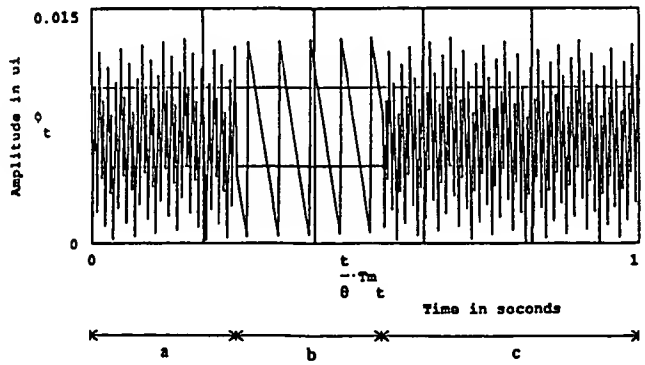


Figure 7 : Jitter in figure 6 for dX = 0

Figure 6 illustrates a case in which the reference clock is tuned to 155 MHz. To observe jitter resulting solely from the difference in phase of the two signals which are assumed stable, let dX = 0 in the expressions (20) and (21). Figure 7 shows jitter represented in figure 6 for dX = 0.

3.2 Jitter filtering

The low-pass filter used for the simulation is represented by the transfer function for a phase locked loop:

$$H(f) = \frac{1}{\left(1 + j\frac{f}{a}\right)^2} \qquad (22)$$

a : cut-off frequency

When the signal is set to 2 Mbit/s and the reference clock tuned to 2 MHz the maximum jitter peak-to-peak is 2 ui. In the case of other plesiochronous sources (8, 34 and 140 Mbit/s) the maximum jitter peak-to-peak is 4, 16 and 68 ui respectively. The problem is now to evaluate the low frequency jitter as it is more difficult to filter.

Figure 8 shows the low frequency envelope (LF) of the jitter from a 140 Mbit/s source and a 2 MHz reference clock. The expression representing the LF envelope of the jitter must now be found.

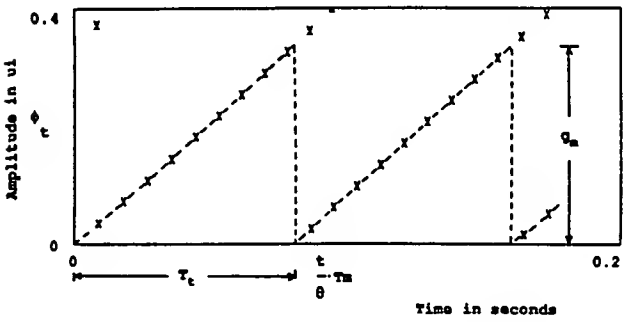


Figure 8 : LF envelope of jitter : g_m = 0.34 ui, T_t = 0.0806 sec

The LF envelope of the jitter is a sawtooth signal (see figure 8) with a slope "ε". Consequently, the relative phase difference expressed in (17) can be represented by :

$$\rho = \frac{h}{k} + \varepsilon \qquad (23)$$

and the additional amplitude in ui provided by "δ" has the value :

$$g_m = \frac{1}{k}\frac{f_a}{H_{ref}} \qquad (24)$$

The period of envelope LF in terms of the number of frames is represented by :

$$N_t = \frac{1}{k\varepsilon} \qquad (25)$$

and the period in seconds by :

$$T_t = N_t \, T_m \qquad (26)$$

Finally, the following expression represents the LF envelope of the jitter in ui :

$$\phi b(t) = \varepsilon t \, \frac{f_a}{H_{ref}} - \left[\frac{1}{k} \, floor(tk\varepsilon)\right] \frac{f_a}{H_{ref}} \qquad (27)$$

The highest additional amplitude (g_m) introduced by the LF envelope must now be found. According to expression (24) the maximum value of g_a results from the smallest value of k and the greatest value of the relation f_a/H_{ref}. The greatest frequency relation (f_a/H_{ref}) results from f_a = 140 Mbit/s and H_{ref} = 2 MHz. For these two frequencies the smallest value of k calculated was 25. The period of the LF jitter envelope will vary depending on the value selected for ε.

Figure 9 shows the variation in the peak-to-peak amplitude of the LF envelope (after filtering via the low-pass filter) according to the frequency of the LF jitter envelope.

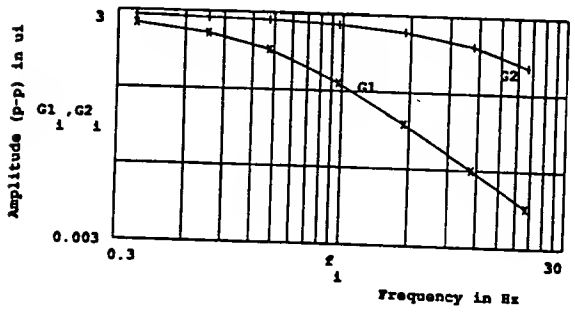


Figure 9 : Amplitude (p-p) of the LF jitter envelope according to frequency.
G1 : graphic with filter cut-off frequency of 1.5 Hz
G2 : graphic with filter cut-off frequency of 15 Hz

Figure 10 shows the amplitude variations according to frequency of the LF jitter envelope (after filtering with filter cut-off frequency of 1.5 Hz). The figure shows the jitter amplitude increasing as the frequency decreases, as the low frequencies are harder to filter. The maximum period of jitter used in the diagram is T_t = 2.76 seconds (frequency: $1/T_t$ = 0.36 Hz). Jitter amplitude peak-to-peak (for the above frequency) is 2.092 ui. The minimum period of jitter used is T_t = 0.09499 seconds (frequency: $1/T_t \approx 20$ Hz). The amplitude of jitter peak-to-peak for this frequency is 0.01 ui (lower than the 1.5 ui specified in G.823). If the filter cut-off frequency is 15 Hz, the amplitude of jitter peak-to-peak is 0.667 ui for frequency of 20 Hz (always lower than 1.5 ui).

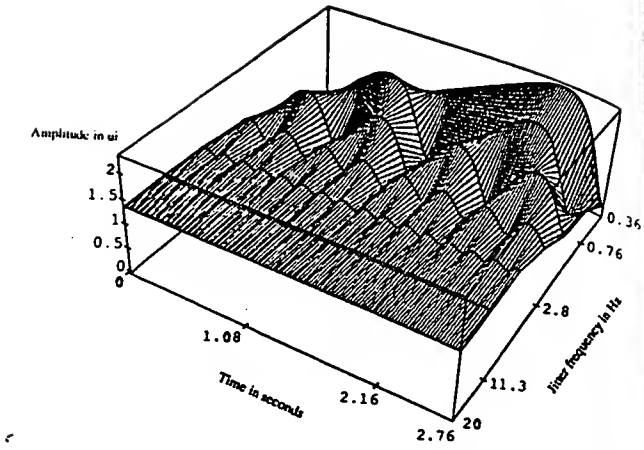


Figure 10 : Variation in LF jitter amplitude according to frequency for cut-off frequency of 1.5 Hz.

4. PROTECTION AGAINST TRANSMISSION ERRORS AND CELL LOSS

In the 2-bytes field reserved for sending clock information the following subfields must be provided :

- the number of bits needed to represent EX
- the number of bits needed to detect and, if necessary, correct transmission errors
- the number of bits needed to correct information lost in the cell.

The value of EX may be represented either by its absolute value or by dX which represents the deviation of EX from its mean value.

If the absolute value of EX is used, errors due to transmission problems or cell loss are corrected during the period (T_a) following the appearance of the error. The receiver counter must be initialised after a delay period long enough for the network transfer time to be taken into account.

In order to detect and correct transmission errors in real time the number of bits used to represent value EX must be reduced. This means using the mean value of EX (EX_0 : cf expression (12)) and value dX (cf expression (13)) and resetting the counter to zero.

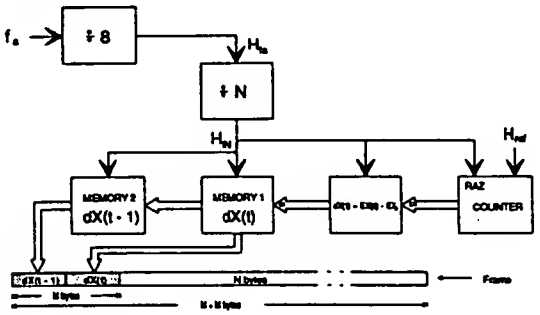
It thus suffices to send the variable dX which will be added on reception to the fixed value EX_0.

Thus, if the reference clock is tuned to 2 MHz (with a tolerance of 50 ppm) the value of EX will vary between 5999 and 6001 (if the absolute value is used the values of EX will be cumulative) while the values of dX will be -1, 0 or 1. It can be seen that in the latter case only 2 bits are needed to represent the value dX so that the remaining bits can be used to protect the information from errors. For the reference clock tuned to 155 MHz (with a maximum tolerance of 20 ppm), the value of dX will vary between -32 and 32, and 6 bits are needed to represent these values.

If the maximum number of bits is 8 to represent dX (the other 8 bits will be used to protect against the cell loss), then we can detect transmission errors.

The cell loss problem remains to be resolved, as if the lost cell contained dX information there will be a fixed phase error. This phase error can be corrected by the receiver phase-locked loop; however, if other cells (containing dX information) are lost before the loop is able to correct it, the phase error will accumulate. To prevent this, phase errors must be corrected as quickly as possible by sending in 1 byte the current value of dX and in the other the previous value of dX in order to verify each time if there has been an error and, if so, to correct it. This method also provides extra protection against transmission errors.

Figure 11 is a schematic diagram illustrating the method at the transmitting end and figure 12 the method at the receiving end.



M = 2 bytes N = 750 bytes

EX_0	:	Mean value of EX
EX(t)	:	Current value of EX
dX(t)	:	Current value of dX
dX(t-1)	:	Previous value of dX
RAZ	:	Reset

Figure 11 : Schematic diagram of transmitter

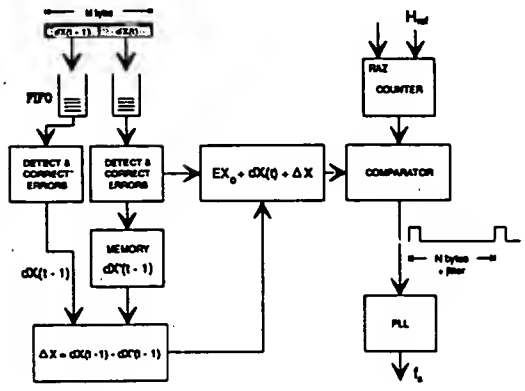


Figure 12 : Schematic diagram of receiver

5. CONCLUSIONS

The performance of a transport network can be measured using several parameters as the end to end error rate, transfert delay or output jitter. The result can be very negative on the service if these parameters are not well managed. The jitter created in a transport network using asynchronous transfer mode can be important and increases with the number of nodes. The proposed method gives a new approach to get rid of the jitter created and its performances are independent of the number of nodes in the network. So using this method the ATM network operator can guarantee jitter specification to the client.

The method presented above, which uses a reference common to both ends, reduces jitter, including waiting time jitter, caused by the ATM network. The need to have a reference common to both ends poses the problem of how to transfer the reference clock. It is possible at present to use the 2 Mbit/s synchronisation network and it will in the future be possible to use the 155 Mbit/s synchronous systems (SDH).

This document shows that both solutions are suitable for all rates in the plesiochronous hierarchy based on the 2 Mbit/s (recommendation G.702). In all the cases studied, residual jitter conforming to the amplitude specified in recommendation G.823.

In addition, this method protects the phase information of the plesiochronous source (dX) against transmission errors and cell loss.

ACKNOWLEDGEMENTS

We would like to thank Mr Thierry Houdoin for his contribution to the design of the method proposed above, Mr Pierre Adam for the fruitful discussions we had together and Mr Jacques Legras for the care he took in reading the manuscript and for the numerous suggestions he made.

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